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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,777	12/13/2001	Edward P. Kuzemchak	TI-32443	6142

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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,777	KUZEMCHAK ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8,10,13 and 15* is/are rejected.

7)☒ Claim(s) *4,5,7,9,11,12,14 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communications filed on 12/13/2001.

Claims 1-16 are pending in the application.

Priority

2. This application files foreign priority under 35 USC 119(a)-(d) to European Application No. 01401752.9, filed Jun. 29, 2001 (TI-32964EU). However, the certified copy of the European Application has not been received.

Oath/Declaration

3. The Oath/Declaration filed on 3/26/02 is objected to:

> It does not state that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in **37 CFR 1.56**.

A new oath/declaration that includes this statement is required.

Specification

4. The blank in page 1, at line 10, in the specification requires updating when the information is available.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 6, 8, 10, 13, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", 1999-ACM.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1: Guerra discloses, "*A method for verifying that two programs are equivalent, the method comprising the steps of:*

executing a first program (See page 964, right column, third full paragraph, C/C++-based cycle-accurate ISA models, see page 967, Figure 4, "Phase1", see page 968, Figure 6(a): <file>.exe)*; collecting a first set of events that are created by the first program while it is being executed* (See page 967, Figure 4, "Phase 1 outputs", see page 968, Figure 6(a))*;*

executing a second program (See page 964, right column, third full paragraph, RTL models, see page 967, Figure 4, "Phase2", see page 968, Figure 6(b): <file>.so)*; collecting a second set of events that are created by the second program while it is being executed* (See page 967, Figure 4, "Phase 2 outputs", see page 968, Figure 6(b))*;*

determining if the first set of events is equivalent to the second set of events by reconciling the first set of events and the second set of events; and indicating the first program is not equivalent to the second program if an unreconciled event is discovered during the step of determining." (See page 964, Abstract, last four lines. See page 968, section 3.4: Debugging)

As per Claim 2: Guerra discloses, "*The method of claim 1, wherein the step of determining comprises the steps of: matching each event of the first set of events to a corresponding event in the second set of*

events; declaring the existence of an unreconciled event if an event in the first set of events does not have a corresponding event in the second set of events; and declaring the existence of an unreconciled event if an event in the second set of events does not have a corresponding event in the first set of events." (See page 967, Figure 4 and page 968, section 3.4: Debugging, particularly referring to VHDL-Based system simulation, VHDL simulator: these features are capable to perform the functions of the claim).

As per Claim 3: Guerra discloses, "*The method of claim 2, wherein: the step of collecting a first set of events comprises developing a logical state for each event of the first set of events* (See page 967, Figure 4, "Phase1 input, write to ISA model", this feature is capable to perform the functions of the claim)*; the step of collecting a second set of events comprises developing a logical state for each event of the second set of events* (See page 967, Figure 4, "Phase 2 inputs, write to ISA model", this feature is capable to perform the functions of the claim)*; and the step of matching comprises comparing the logical state of each event of the first set of events to the logical state of the corresponding event in the second set of events*" (See section 3.4, Debugging and referring to "simulation").

As per Claim 6: Guerra discloses, "*The method of claim 1, wherein the step of indicating comprises activating the debugging capability in the software development system executing a first program at the point where the unreconciled event is discovered and activating the debugging capability in the software development system executing a second program at the point where the unreconciled event is discovered.*" (See page 968, Section 3.4 Debugging, particularly see Figure 6).

As per Claim 8: Guerra discloses, "*The method of claim 1, wherein: the steps of collecting a first set of events and collecting a second set of events comprise treating references to address registers in instructions as symbols; and the step of determining comprises computing the effective addresses of the analogous references in the first set of event and the second set of events when reconciling the first set of events and the second set of events.*" (See Figure 6, "Compiler"; where a compiler is capable to *treat references to address registers in instructions as symbols;* See page 966, section 2.3, "using instruction-accurate approach", "pipeline", "decode stage" etc., having the capability to *determine computing the effective addresses*).

As per Claim 10: Guerra discloses, "*The method of claim 1 wherein the steps of collecting a first set of events and collecting a second set of events comprise: determining that a first instruction is in the instruction pipeline; calculating the current effective address delay of the instruction in the pipeline; finding that a valid effective address for the instruction is available based on the current effective address delay of the instruction; computing the effective address of the first instruction if a valid effective address is not available; and reporting the effective address of the instruction.*" (See page 966, section 2.3, Figure 2, Figure 3, having the capability to determine, calculate, compute, and report as claimed).

As per Claim 13: Guerra discloses, "*The method of claim 1, wherein the means for executing, collecting, determining, and indicating is a first verification program whereby the verification program causes a first program to be executed by a first software development system, causes a second program to be executed by a second software development system, and receives information from the first software development system and the second software development system to perform the steps of collecting, determining, and indicating.*" (See page 968, section 3.4, and particularly, diagrams of Figures 6(a) and (b)).

As per Claim 15: Claim 15 is claiming a system, where the claim has the limitation corresponding to functionality performed by the method recited in Claim 1. Claim 15 is rejected in the same reason set forth in connecting to the rejection of Claim 1.

Allowable Subject Matter

7. Claims 4 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior art of record, Guerra, and cited prior arts of record, alone or in combination, do not disclose "*wherein the steps of executing a first program, collecting a first set of events, executing a second program, collecting a second set of events, and determining are performed in a iterative manner such that: after executing the first program and collecting a first event, execution of the first program is halted;*

the steps of executing the second program, collecting the second set of events, and determining are performed until an event in the second set of events is found that corresponds to the first event collected; the steps of executing the first program, collecting a first set of events, and determining are performed until events in the first set of events are found that correspond to all events in the second set of events and at least one event remains in the first set of events; and the steps of executing the second program, collecting a second set of events, and determining are performed until events in the second set of events are found that correspond to each event in the first set of events." as recited in Claim 4 and in such manner in Claim 16.

8. Claims 5, 7, 9, 11-12, and 14: The claims are objected to because the claims are depended on Claim 4, which is objected to as above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fritz, US 5,949,993, discloses a method for generating a hardware/software development tool including ISA simulators and assemblers.

Levitt et al., "A Scalable Formal Verification Methodology for Pipelined Microprocessors", discloses verification techniques involving in a pipeline and a deconstructing pipeline.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on 8:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TED T. VO

TTV
Patent Examiner
Art Unit 2122
August 20, 2004